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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,482	02/06/2004	Jerome Bombal	TI- 34796	7063

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EXAMINER	
KRAVETS, LEONID	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,482	BOMBAL, JEROME	
	Examiner	Art Unit	
	Leonid Kravets	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Priority

1. Examiner acknowledges applicant's request for priority to European application EP3291984.

Information Disclosure Statement

2. Examiner acknowledges receipt of information disclosure statement dated 5/27/2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-9 and 11-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hattori (US Patent 5,521,876).

5. As per claim 1, Hattori discloses an electronic device, comprising:

an input for receiving successive data words, wherein each data word of the successive data words comprises a plurality of bits (Col 7, Lines 41-43);

a memory structure comprising a plurality of memory word addresses, wherein each memory word address corresponds to a storage structure operable to store a data word having the plurality of bits (Col 7, Lines 47-52);

control circuitry, operable during a non-overflow condition of the memory structure, for writing successive ones of received data words into respective successive ones of the memory word addresses [X pointer points to column and Y pointer points to a row, X pointer moves from 0 to m in sequence, until it reaches m. At this point, the row overflows and Y is incremented (Col 7, Lines 47-59)]; and

control circuitry, operable during an overflow condition of the memory structure, for writing each data word in successive ones of received data words across multiple ones of the memory word addresses [The words will continue to be written across multiple memory word addresses (rows) when Y is incremented (Col 7, Lines 47-59)].

As per claim 2, Hattori discloses the electronic device of claim 1 wherein the control circuitry, operable during an overflow condition of the memory structure, is for writing each data word in the successive ones of received data words across a same set of the multiple ones of the memory word addresses [All words of Hattori are written across a same set of the memory word addresses, namely addresses 0 to m of each row (Col 7, Lines 52-53)].

As per claim 3, Hattori discloses the electronic device of claim 2: wherein the plurality of bits consists of an integer number N of bits; and wherein N is selected from a

group consisting of 128, 64, 32, 16, 8, and 4 [The device of Hattori provides an 8 bit bus to each memory cell, thus each cell must be able to store words 8 bits wide, combining the cells allows storage of larger words. Further, selection of the width of the memory is a design choice as it is known in the art to vary the memory width (Col 6, Lines 1-7)].

As per claim 4, Hattori discloses the electronic device of claim 1 wherein the control circuitry, operable during an overflow condition of the memory structure, is for writing each data word in the successive ones of received data words across a same set of multiple contiguously-addressed ones of the memory word addresses [All words are written into the same set of contiguously-addressed addresses pointed to by pointer Y from 0 to k (Col 7, Lines 47-59).

As per claim 5, Hattori discloses the electronic device of claim 1 and further comprising circuitry for detecting the overflow condition (Col 7, Lines 53-55).

As per claim 6, Hattori discloses the electronic device of claim 5 wherein the circuitry for detecting the overflow condition is responsive to detecting a potential write of a data word into one of the memory word addresses, wherein the one memory word address already stores an unread data word [The system of Hattori must have stored unread data word since it has just written into this row, hence increasing the Y pointer (Col 7, Lines 53-55)].

As per claim 7, Hattori discloses the electronic device of claim 1 and further comprising circuitry for reading data words written during the non-overflow condition (Col 8, Lines 18-21).

As per claim 8, Hattori discloses the electronic device of claim 7 and further comprising circuitry for reading data words written during the overflow condition (Col 8, Lines 18-21).

As per claim 9, Hattori discloses the electronic device of claim 8 wherein the circuitry for reading data words written during the overflow condition comprises circuitry for reading each data word from multiple contiguously-addressed ones of the memory word addresses (Col 8, Lines 18-21).

As per claim 11, Hattori discloses the electronic device of claim 1 wherein the successive data words represent data selected from a group consisting of audio, screen trace, bit map, and uncompressed video data (Col 10, Lines 50-51).

As per claims 12-15, please see rejection of claims 1-4 above.

As per claims 16-19, please see rejection of claims 6-9 above.

As per claim 20, please see rejection of claim 11 above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori.

As per claim 10, Hattori discloses the electronic device of claim 1 wherein the memory structure, the control circuitry operable during a non-overflow condition of the memory structure, and the control circuitry operable during an overflow condition. Hattori does not disclose that they are all part of a handheld computing device.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the memory device of Hattori into a handheld computing device since the device would allow for portable computers to achieve the benefits of Hattori, such as relieving the host CPU of its work load (Col 2, Lines 51-54).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent to Qureshi (5,974,516) describes writing to a FIFO in two-dimensions

Patent to Cundorelli (6,556,495) describes writing to a two-dimensional FIFO having translations and offsetting.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Kravets whose telephone number is 571-272-2706. The examiner can normally be reached on Mon-Fri 8-430.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on 571-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonid Kravets
Patent Examiner
Art Unit 2189

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

March 28, 2006